What is claimed is:

1. A signal deconstruction circuit for use in an RF transmitter and configured for complementing modulation circuitry of said transmitter for digitally generating a non-constant envelope modulation signal, said deconstruction circuit comprising a digital signal processor configured for deconstructing a resultant signal having an undesirable property into one or more deconstruct signals which do not have said undesirable property, whereby signals derived from said deconstruct signals are subject to conversion to analog signals, processing by power efficient, dynamic-range limited analog circuits and recombination.

2. A circuit according to claim 1 wherein said undesirable property is a relatively high peak-to-average power ratio.

3. A circuit according to claim 2 wherein said modulation circuitry comprises an Inverse Fourier transform processor and said deconstruction circuit is operative on said resultant signal after said Inverse Fourier transform processor.

4. A signal deconstruction circuit for use in an RF transmitter and configured for complementing modulation circuitry of said transmitter for digitally generating a non-constant envelope modulation signal, said deconstruction circuit comprising a digital signal processor configured for deconstructing a resultant signal having an undesirable property into a plurality of deconstruct signals which do not have said undesirable property.

5. A circuit according to claim 4 wherein said undesirable property is a relatively high peak-to-average power ratio.

6. A circuit according to claim 5 wherein said modulation circuitry comprises an Inverse Fourier transform processor and said deconstruction circuit is operative on

said resultant signal prior to said Inverse Fourier transform processor.

7. A circuit according to claim 5 wherein said modulation circuitry comprises an Inverse Fourier processor and said deconstruction circuit is operative on said resultant signal after said Inverse Fourier transform processor.

8. A circuit according to claim 6 comprising a carrier-sorting engine and said modulation is OFDM.

9. A circuit according to claim 8 wherein said carrier-sorting engine sorts carriers of said resultant signal into a plurality of groups, each said group forming one said deconstruct signal whereby said modulation circuitry comprises a plurality of Inverse Fourier transform processors for transforming said deconstruct signals, each said Inverse Fourier transform processor being smaller than would be required to transform said resultant signal without said deconstruction of the same into said deconstruct signals.

10. A circuit according to claim 9 wherein said carriers are simultaneously sorted in more than one way to produce a plurality of alternative deconstruct signals for each said group, whereby said deconstruct signals are selected from one said group on the basis of having the best peak-to-average power ratio.

11. A circuit according to claim 7 comprising a phasor fragmentation engine.

12. A circuit according to claim 11 wherein said phasor fragmentation engine deconstructs said resultant signal into a plurality of equal, varying amplitude deconstruct signals the phasors of which combine to form a phasor corresponding to said resultant signal, wherein said amplitude of said deconstruct signals is a predetermined proportion of the variation of the amplitude of said resultant signal about the mean amplitude thereof.

13. A circuit according to claim 12 wherein said phasor fragmentation engine deconstructs said resultant signal into two equal, varying amplitude deconstruct signals, said deconstructing comprising converting sequences of complex time samples output from said Inverse Fourier transform processor into two parallel sequences of equal magnitude phasor at two phases whereby said phases are calculated to be $\theta - \Phi$ and $\theta + \Phi$, respectively, whereby $\Phi = \cos^{-1}(0.5V / V_{PHASOR})$ wherein V is the amplitude of the current sample of said resultant signal and V_{PHASOR} is the amplitude of said deconstruct signals calculated to be $K_1 V - K_2$ wherein K_1 and K_2 are constants.

14. A circuit according to claim 11 wherein said phasor fragmentation engine deconstructs said resultant signal into a plurality of equal and constant amplitude deconstruct signals.

15. A circuit according to claim 14 wherein said resultant signal is preconditioned by a second deconstruction circuit.

16. A circuit according to claim 15 wherein said second deconstruction circuit comprises a carrier sorting engine.

17. A circuit according to claim 15 wherein said second deconstruction circuit comprises a preconditioning phasor fragmentation engine for preconditioning a second resultant signal prior to said processing of said resultant signal, wherein said preconditioning phasor fragmentation engine deconstructs said second resultant signal into a plurality of equal but varying amplitude preconditioned deconstruct signals the phasors of which combine to form a phasor corresponding to said second resultant signal, wherein said amplitude of said preconditioned deconstruct signals is a predetermined proportion of the variation of the amplitude of said second resultant signal about the mean amplitude thereof.

18. A circuit according to claim 15 wherein said phasor fragmentation engine is configured for converting sequences of complex time samples output from said Inverse Fourier transform processor into two parallel sequences of two equal magnitude phasors, equal to Vmax/2, at two phases, whereby said phases of said two equal magnitude phasors are calculated to be $\theta - \Phi$ and $\theta + \Phi$, respectively, whereby $\Phi = \cos^{-1}(V / Vmax)$ wherein V is the amplitude of the current sample of said resultant signal and Vmax is the maximum amplitude of said resultant signal over the period of said sequence.

19. A circuit according to claim 14 wherein said phasor fragmentation engine is configured for converting sequences of complex time samples output from said Inverse Fourier transform processor into three parallel sequences of three equal magnitude phasors, equal to Vmax/3, at three phases, whereby said phases of two said equal magnitude phasors are calculated to be $\theta - \Phi$ and $\theta + \Phi$, respectively, and said third phase is equal to the phase of said resultant signal, whereby $\phi = \cos^{-1}[(1.5\ V / V_{MAX}) - 0.5]$, V being the amplitude of the current sample of said resultant signal and Vmax being the maximum amplitude of said resultant signal over the period of said sequence.

20. A circuit according to claim 3 comprising a virtual range-hopped engine configured for shifting a peak signal output from said Inverse Fourier transform processor to time samples targeted for attenuation by a preselected windowing function.

21. A circuit according to claim 15 wherein said second deconstruction circuit comprises a light windowing engine.

22. A circuit according to claim 15 further comprising an amplitude and phase comparison calibration circuit for adjusting differences in channel gains and phases between said deconstruct signals when combined following parallel up-

converter/power amplifier chains to regenerate a modulated waveform, said calibration circuit comprising an error signal generator for generating error signals configured for adjusting said regenerated waveform.

23. A circuit according to claim 19 wherein said modulation is OFDM.

24. A circuit according to claim 23 further comprising an amplitude and phase comparison calibration circuit for adjusting differences in channel gains and phases between said deconstruct signals when combined following parallel up-converter/power amplifier chains to regenerate a modulated waveform, said calibration circuit comprising an error signal generator for generating error signals configured for adjusting said regenerated waveform.

25. A signal deconstruction method for complementing the generation of a digitally generated non-constant envelope modulation signal in an RF transmitter, said method comprising deconstructing a resultant signal having an undesirable property into a plurality of deconstruct signals which do not have said undesirable property whereby signals derived from said deconstruct signals are subject to conversion to analog signals, processing by power efficient, dynamic-range limited analog circuits and recombination.

26. A method according to claim 25 whereby said undesirable property is a relatively high peak-to-average power ratio.

27. A method according to claim 26 whereby said modulation signal is generated using an Inverse Fourier transform processor and said deconstructing is performed prior to modulation by said Inverse Fourier transform processor.

28. A method according to claim 26 whereby said modulation signal is generated using an Inverse Fourier transform processor and said deconstructing

is performed subsequent to modulation by said Inverse Fourier transform processor.

29. A method according to claim 27 whereby said deconstructing comprises sorting carriers of said resultant signal into a plurality of groups, each said group forming one said deconstruct signal, whereby said modulation is performed by a plurality of Inverse Fourier transform processors for transforming said deconstruct signals, each said Inverse Fourier transform processor being smaller than would be required to transform said resultant signal without said deconstructing step.

30. A method according to claim 29 whereby said carriers are simultaneously sorted in more than one way to produce a plurality of alternative deconstruct signals for each said group and selecting said deconstruct signals for one said group on the basis of having the best peak-to-average power ratio.

31. A method according to claim 28 whereby said resultant signal is deconstructed into a plurality of equal, varying amplitude deconstruct signals the phasors of which combine to form a phasor corresponding to said resultant signal, wherein said amplitude of said deconstruct signals is a predetermined proportion of the variation of the amplitude of said resultant signal about the mean amplitude thereof.

32. A method according to claim 31 wherein said resultant signal is deconstructed into two equal, varying amplitude deconstruct signals and said deconstructing comprising converting sequences of complex time samples output from said Inverse Fourier transform processor into two parallel sequences of equal magnitude phasors, equal to Vmax/2, at two phases whereby said phases are calculated to be $\theta - \Phi$ and $\theta + \Phi$, respectively, whereby $\Phi = \cos^{-1}(0.5V / V_{PHASOR})$ wherein V is the amplitude of the current sample of said resultant signal and V_{PHASOR} is the amplitude of said deconstruct signals calculated to be $K_1 V - K_2$

wherein K_1 and K_2 are constants.

33. A method according to claim 28 whereby said resultant signal is deconstructed into a plurality of equal and constant amplitude deconstruct signals.

34. A method according to claim 33 whereby said resultant signal is deconstructed into two said deconstruct signals and said resultant signal is preconditioned by deconstructing a second resultant signal into a plurality of equal but varying amplitude preconditioned deconstruct signals the phasors of which combine to form a phasor corresponding to said second resultant signal, wherein said amplitude of said preconditioned deconstruct signals is a predetermined proportion of the variation of the amplitude of said second resultant signal about the mean amplitude thereof.

35. A method according to claim 33 comprising converting sequences of complex time samples output from said Inverse Fourier transform processor into three parallel sequences of three equal magnitude phasors, equal to Vmax/3, at three phases, whereby said phases of two said equal magnitude phasors are calculated to be $\theta - \Phi$ and $\theta + \Phi$, respectively, and said third phase is equal to the phase of said resultant signal, whereby $\phi = \cos^{-1} [(1.5\ V / V_{MAX}) - 0.5]$, V being the amplitude of the current sample of said resultant signal and Vmax being the maximum amplitude of said resultant signal over the period of said sequence.

36. A method according to claim 28 comprising shifting a peak signal output from said Inverse Fourier transform processor to time samples targeted for attenuation by a preselected windowing function.